

WHAT IS CLAIMED IS:

- 1 1. A CMOS pixel for use in a CMOS imager, comprising:..
 - 2 a. a photodiode having a substantially square-shaped image
 - 3 sensing area, an anode coupled to ground and a cathode;
 - 4 b. a transfer transistor having a drain coupled to the cathode of the
 - 5 photodiode, a gate controlled by a control signal, Tx, and a source coupled to a floating
 - 6 sensing node;
 - 7 c. a reset transistor having a drain coupled to a reset potential, a
 - 8 gate controlled by a control signal, Rx, and a source coupled to the floating sensing node; and
 - 9 d. a source follower coupled between the floating node and an
 - 10 output of the unit pixel, the source follower controlled by a select signal.
- 1 2. The CMOS pixel of claim 1, wherein the source transistor, reset
- 2 transistor and source follower are positioned along at least two sides of the image sensing
- 3 area.
- 1 3. The CMOS pixel of claim 1, further comprising a substantially
- 2 hemispherically-shaped microlens positioned substantially over the image sensing area.
- 1 4. An array of CMOS pixels, each pixel comprising a substantially square
- 2 image sensing region, wherein a distance between the image sensing regions of neighboring
- 3 pixels is optimized to reduce crosstalk between the neighboring pixels.
- 1 5. The array of pixels of claim 4, wherein the distance is further
- 2 optimized to improve MTF.
- 1 6. An improved CMOS imaging array for use in a CMOS imaging
- 2 system, the improvement comprising:
 - 3 using a substantially square image sensing region within each pixel to
 - 4 reduce the distance between the image sensing regions of neighboring pixels.
- 1 7. The CMOS imaging array of claim 6, further comprising: a microlens,
- 2 positioned over the image sensing area of each pixel to increase the effective fill factor.
- 1 8. The CMOS imaging array of claim 7, wherein each pixel comprises:

2 a. a transfer transistor having a drain coupled to the cathode of the
3 photodiode, a gate controlled by a control signal, Tx, and a source coupled to a floating
4 sensing node;

5 b. a reset transistor having a drain coupled to a reset potential, a
6 gate controlled by a control signal, Rx, and a source coupled to the floating sensing node; and

7 c. a source follower coupled between the floating node and an
8 output of the unit pixel, the source follower controlled by a select signal.